eSeminar Q&A for Challenges of Differential Bus Design (Feb. 20, 2002)

Q: I am familiar with the older RS-422, RS-423, and RS-485 differential bus standards. Is there a newer prevailing standard?
A: No, I don't really know if there is a newer standard or not.

Q: What are the units on the bottom of the plots on slides 15 and 16 (differential impedance vs. time) of the presentation?
A: My apologies on leaving that out. Those are in nanoseconds. On the eye diagrams in slides 19, 20, 23, and 26 the units on those are picoseconds.

Q: Referring to slides 15 and 16 (differential impedance), assuming that the X axis is time, how do you get a slope when there is no capacitance in the circuit?
A: The slope comes from a series R. Remember, a TDR sends this edge down this transmission line that we are measuring, in this case the transmission line is ten inches long, propagation is probably about 180 picoseconds per inch. As it moves down it feels this impedance but it also sees the series R and the series R adds directly to the perceived impedance on this pulse and is reflected back that way. If you build this model, make that series R go to 0 and you will see that those lines become flat.

There is also a second order effect here. If you plot these out and you turn the plot sideways and sight down the edge you will see it's not perfectly flat. I believe this is due to that as this edge propagates down this transmission line, it begins to slow down due to the dielectric losses and metal and skin effect kinds of losses. With the fastest edge we have the highest frequency components, this current crowding -- the skin effect, is aggravated. You recall a skin effect is a frequency dependent kind of thing. And the higher the frequency, the thinner the skin that gets generated.

The effect of resistance of this trace seems to be just a little bit higher because the current is crowded into a part of the metal and so it doesn't get to see the entire cross-section of the trace. So build this model in ADS if you have it there. If you get a demo version, play with it here. I think you will see that this is kind of what happens. It's a fun thing to do.

Q: How many traces and layers in a complex board stackup can you simulate with the ADS multilayer tools?
A: In terms of the substrate definition, currently I believe it's 40 layers (there are pre-defined substrates for 1 through 10 layers, and 12, 14,16, 32 and 40) and there are provisions to go up to 255. In terms of number of traces, the total number of traces is really unlimited. The number of traces that you can simulate as an entire group the maximum is 16. But there is a grouping function that will allow you to group five of those, so that's five times 16, or 80. That means that you can simulate that set and simulate the interaction between one trace and every other trace in there. So it's a very complex kind of thing. It also makes the simulation time go up, so you need to be kind of careful how you do that. I generally try not to use those complex functions except at the very last, just before the entire model is delivered. There is an ADS presentation titled "Multilayer Interconnect Library Extension" which illustrates how to extend the list of substrates up to 255 at http://contact.tm.agilent.com/tmo/eesof/products/e9008a-b.html#Applications. The tradeoff in doing this is that the simulation time increases for every substrate layer.

Q: The differential impedance that is continually referenced seems to be more of an odd mode impedance. Is that accurate?
A: Yes. Some call it even mode and odd mode. I like differential and common mode, but you are right.

Q: What is the common mode voltage?
A: The common mode voltage is (Vpos+Vneg)/2.

Q: I'm not familiar with the ADS simulator. Where can I get more information on the ADS simulator?

A: There is a URL for ADS on the resource page (slide 43 of the seminar), http://www.agilent.com/find/eesof-eda, just click on that. Your local Agilent sales representative can provide you with more information.

Q: Do I input driver and receiver models for ADS in IBIS format? Is this model sufficient?

A: When I was talking about importing driver models, I'm really talking about coming in from HSpice typically or PSpice or some other Spice simulator. It would be very much a transistor level kind of model. My experience is that is the best way to go because that's what the silicon designers are using. Anything other than that, there are some compromises. I think they can be worked out really well, but because ADS will import HSpice stuff quite well, that's what I recommend.

Q: Can you explain how differential mode impedance interacts with single ended impedance? For a 50 ohm single ended transmission line when it's coupled to a differential trace with 50 ohm single ended impedance and 120 ohm differential impedance, will we see a reflection? What single ended and differential impedance values eliminate that reflection?

A: This is a great question for demonstrating the need for a good simulator. This is part of the reason that people want to start out designing differential traces with loosely coupled differential pairs. In this case the differential impedance and the single-ended impedance are just a two-to-one ratio. And it's fairly easy. But as you start pushing things together to get higher signaling density, higher trace routing density, then the differential impedance no longer is an integer relationship with the single ended impedance. And it becomes somewhat tricky.

Because your desired signal is differential, you will want to terminate that on both ends because that is going to be the highest amplitude by definition, that's what you want. But then what happens to the single ended because that won't match? You can build somewhat complex networks that have different common mode termination versus differential termination and that's often too complex a solution. I think what most people do is to use the simulator, terminate differentially first, and then see what the penalty will be as you generate a single-ended signal in the simulator and what happens when it is not terminated ideally? I think that's the way to go. There will be some compromises here, so that's often the one I think that people will make.

Q: Does ADS allow for frequency dependent dielectric constants or are you limited to a fixed value?

A: Yes. ADS can accommodate the dielectric constant (and other variables) being a function of frequency. Simply make the dielectric constant a variable, and place the desired equation in a Variable block. ADS reserves the variable name "freq" to refer to frequency. Note the equation can be closed form, or it can be piece-wise linear. Or you can make the variable be a data access component that looks up data from an ADS dataset. For data to be imported to a dataset, it would have to read in as a CITIFILE or an MDIF file format.

Q: When you were talking about the driver and reflected signals, you didn't talk about source termination. Can you comment on that?

A: Source termination is one of the critical things in dealing with the reflections. Even LVDS drivers are current sources, so they don't deal with reflections really well as a signaling source. But part of this termination discussion, part of the termination is often tied up in the transistors themselves and so for that reason if things are really tight, I'm recommending that people import their drivers into ADS and get a more accurate understanding of what happens.

But part of the concern here is that often a driver will be designed to have a good 50 ohm output impedance or 100 ohm differential, if that's what your goal is, over the desired output range but when the reflections come back and push the driver outside this range, it's no longer specified to be 50 ohm output impedance or whatever its impedance is or 100 ohm differential. And that really becomes the concern of the whole reflection thing. What happens when the reflection comes back, it overshoots the driver, instead of looking like 100 ohms differential, it begins to look like 120 ohms or 80 ohms. That's where you need to a good simulator and approach this methodology to make it work.

Q: If you run differential signals in two separate single mode impedance traces, what is the most important factor to consider in the trace routing?

A: Routing differential signals as two single traces is what I call loosely coupled differential pairs where there is very little coupling between the two signals. You still get most of the benefits of differential signaling, the ground cancellation, the ground return current cancellation, the other kinds of things. What I recommend to layout people when they are routing these kinds of signals is to pick a constant spacing and to run them pretty much as though they are differential pairs. And some people will say you can run them most anywhere, you can run one part of a signal on this side of the board and one on the other side of the board. I would recommend not doing that.

Q: You identified several different differential layout topologies in slide 12 but did not really make a recommendation. Do you have a recommendation?
A: No, I don't have a recommendation. I recommend starting with the standard edge, loosely edge-coupled and then beginning to go from there. The reason I don't have a recommendation is that every system seems to be so different. For some systems the really difficult problem is crowding these thousands of signals into this small area. For some systems the real difficult part is signal precision. This may be a test system at the far end you want very precise amplitudes and the overshoot can be no more than just a few millivolts. You would have pretty much different requirements for each of those. But I think starting with kind of an edge-coupled is probably the way to go.

Q: Where is the ground contact in the measurement setup photo of the probe on slide 34?
A: On slide 34 we see the point of the probe. In this case it's hard to see because it's a narrower pitch probe. I apologize for not having enough resolution on that, I think it's partly disappeared in the pixelation but there is one there. With the narrower pitch probes it's pretty hard to see to separate the ground and the signal.

Q: What has been your experience with the new Agilent four port network analyzers?
A: That's an exciting product that's just recently come out. For the differential bus, for looking at complex kinds of structures now, there is just nothing better than that. I've found it takes a little while to get the calibration down and to become familiar with that but it has some really nice features, really nice software to convert from frequency to time domain that is pretty sophisticated. And allows a lot of different things to be done.

Q: What's the upper frequency range related to ratio of the trace width to the thickness of the substrate that the ADS model is still good when compared to measurement data?
A: I haven't experimentally pushed that limit. I believe fundamentally that it should be good for virtually any kind of practical ratios because the multi-layer suite set of models really solves Maxwell's equations. My understanding is that it's not an equation based curve fitting but it really goes in and solves the fundamental equations every time.

Q: What are the disadvantages of using broadside closed coupling?
A: First of all, it's probably unusual. I think it will be used more in the future. As you begin to bring traces closer and closer together, the fields begin to exist just in that range in electric fields, so there will be more current crowding in there. So there may be more dielectric loss and more metal loss. I think that's one of the trade-offs that has to be made.

Q: The 8720ES network analyzer does single ended calibration. Is there a way to calibrate it differentially, that is using a PCB with differential traces?
A: No, unfortunately I don't know of any way to do that. I have heard of tricks where people have purchased baluns and done things, but that kind of works for narrow band for maybe a microwave purpose. There are differential network analyzers available, Agilent has recently offered those. That would be the way to go if you want to have a differential analyzer.

Q: Can you use a single-ended network analyzer in the differential mode?
A: Yes. A recent eSeminar titled "RF Balanced Device Characterization", presented on Jan. 15, 2002, describes this technique and the systems involved. You can access the eSeminar at http://www.netseminar.com/guestbook/showSeminar?sem_num=571.

Q: Would you comment on how to terminate the differential bus if there are modal conversions on the traces from differential to common mode?

A: I guess that depends on the degree of conversion. The starting point seems to be is to terminate differential mode at its differential impedance. There are also some tricks to be played with altering the differential impedance to maximize the received signal at the expense of generating some reflections going back to the driver. If there is a lot of conversion, once you start having traces crowded closely together the crosstalk will be part differential mode, and part common mode, so there is always this kind of mix of these signals here. My experience has been is that if the common mode signal is relatively low, that the differential mode impedance is probably good enough.

You may also be asking about when you put a resistor from the positive to the negative. That's a differential termination, but it doesn't terminate the common mode at all. If you connect, you know, resistor from trace to ground on each of those, then you begin to terminate both common mode and differential.

Q: I need something which can measure the Return Loss or Input Impedance vs. Frequency easily for our products which have either 100 or 120 differential twisted pair input impedance, or a 75 Ohm unbalanced input option. Due to all the surge protection components we need to validate our input impedance per ITU-T Recommendations (~ 26 dB return loss over frequency). Can you recommend a solution?

A: Any network analyzer capable of measuring mixed-mode S-parameters would work well for this application. They can handle the transformation to non-50-ohm impedances and do balanced and unbalanced measurements. A good choice is the Agilent E5070A to 3 GHz or the E5071A to 8.5 GHz.

Q: This is interesting, but is it relevant to semiconductor chip design?

A: The relevance is that every chip needs to talk to the outside world. As the data rates increase, the chip I/O design is now merging with the interconnect design, because these two signaling aspects strongly interact with each other. This includes traditional signal integrity items, such as impedance, reflections, timing, and cross talk, but also includes signal conditioning, such as pre-emphasis and receiver equalization.

Q: When will ADS offer IBIS compatibility that you had on MDS?

A: At this point in time this capability is not available with ADS. Please contact your Agilent EEsof EDA representative to see when it might be available.

Q: I would be very interested in a seminar on TDR fundamentals and applications. Can you recommend anything?

A: There isn't a specific seminar on TDR, but there are several resources available from the Agilent website. Please refer to the Application Central page for TDR at http://www.measurement.tm.agilent.com/new/category713.html

Q: I am a new electrical engineer and am looking to learn as much about the complexity of designing highly sophisticated circuit boards. What do you recommend?

A: There are several resources such as training seminars and books to aid you in high-speed digital PCB design. GigaTest Labs and the Copper Connection provide periodic seminars. A common reference book is "High-Speed Digital Design: A Handbook of Black Magic" by Howard Johnson. And of course, TechKnowledge is available for consulting.

Q: Can I get a copy of the presentation?

A: Yes, go to slide 43 of the eSeminar archive. From there you can get a copy of the presentation plus find many valuable links for more information on the subject. There is also a Router & Switch discussion forum link (http://www.agilent.com/find/forums) if you would like to pose/review other questions.